Non-Volatile Memories: A Look into the Future

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Moore's Law in NV Memory

- Moore's Law will continue through innovation
  - Process complexity will increase to address fundamental limits of physics
- To maintain Moore's Law cost learning curve, difficult to do it by transistor technology alone
  - New opportunity for new memory structures and new materials
- Current mainstream NV memory technologies of ETOX and NAND will continue to be the key technologies for more than 5 years out
- Intense research activities to identify scalable memory technologies for 5 year and beyond

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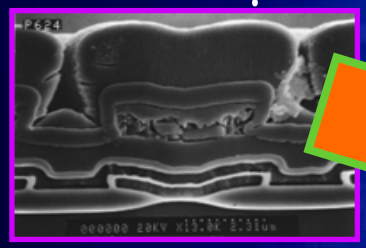
Moore's Law will Continue with ETOX® Flash

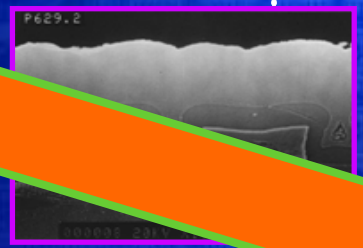
- Currently shipping 8th generation of ETOX® flash memory in high volume and ready to ship at 90nm
  - ~50% cell size reduction per generation
- Good visibility to 65 nm and 45 nm generations
- Further innovation required to maintain cost learning curve

Intel ETOX® (NOR) Technology Scaling

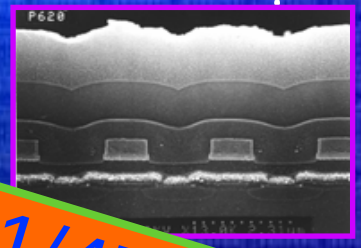
1986 / 1.5µm



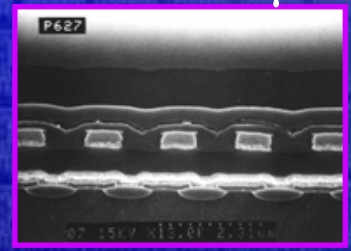
1988 / 1.0µm



1991 / 0.8µm



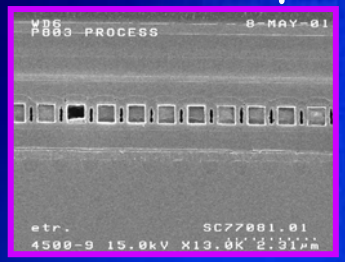
1993 / 0.6µm



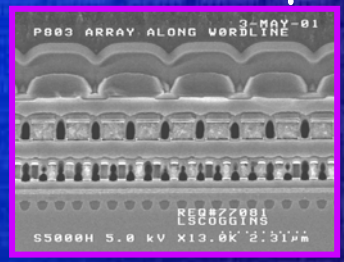
1996 / 0.4µm

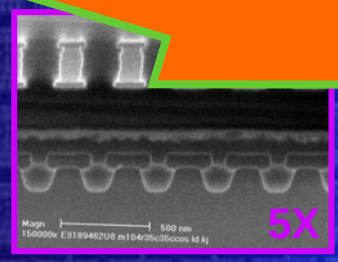
1/476

1998 / 0.25µm

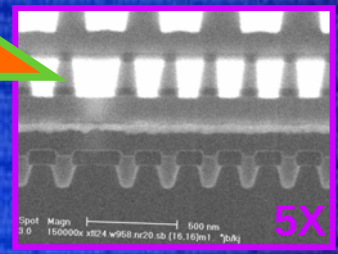


2000 / 0.18µm





2004 / 90nm

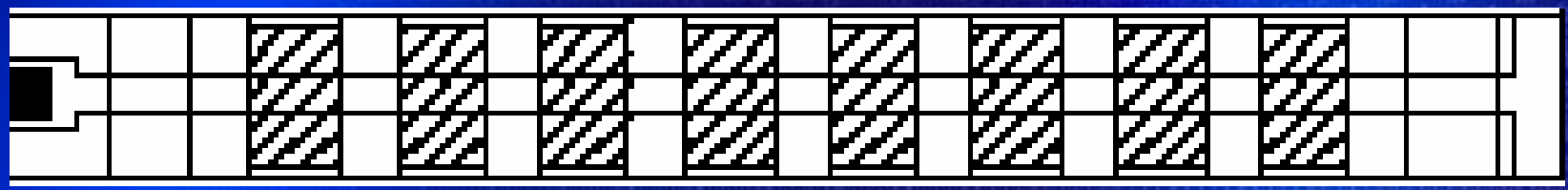


Volume Production Year / Technology Generation

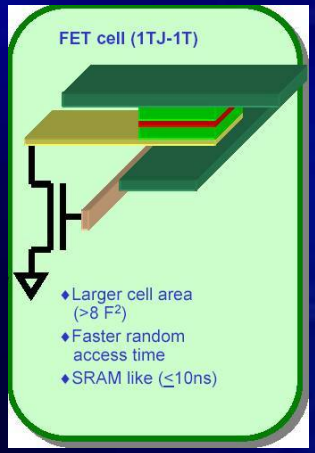
- **16+ years & 8 Generations of ETOX® (Intel NOR) High Volume Production to 0.13 µm**
- **5+ years and 4 Generations of Intel StrataFlash™ (Multi Level Cells 2bit / cell) memory**

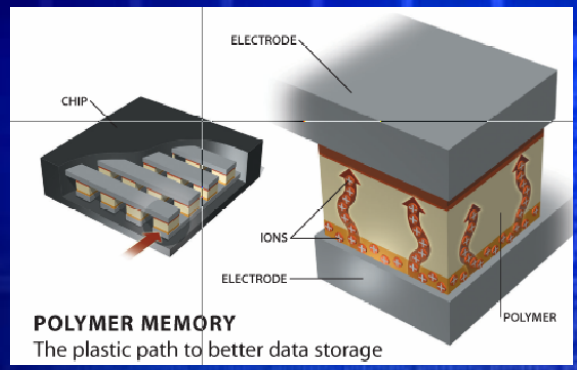
NAND Memory

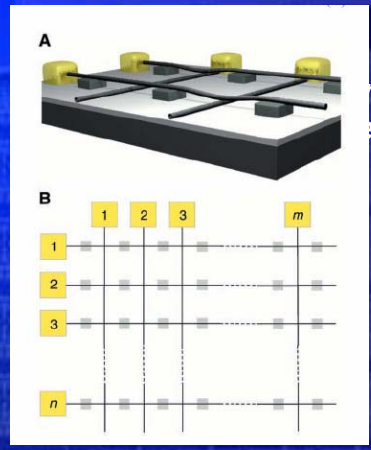
- NAND cell layout is close to litho defined minimum ~ 4 to 5 λ^2
- 2 bit per cell reduced effective cell size by half
- Good visibility to the next couple of generations
- 2 bit per cell NAND will be the lowest cost NV memory for the rest of this decade

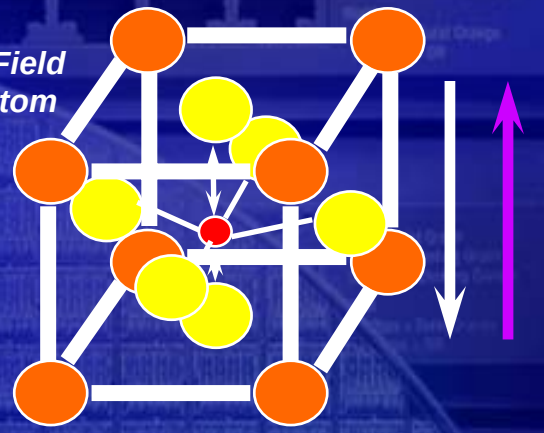


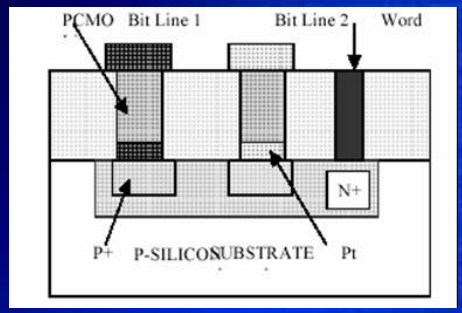
Examples of new memory technologies

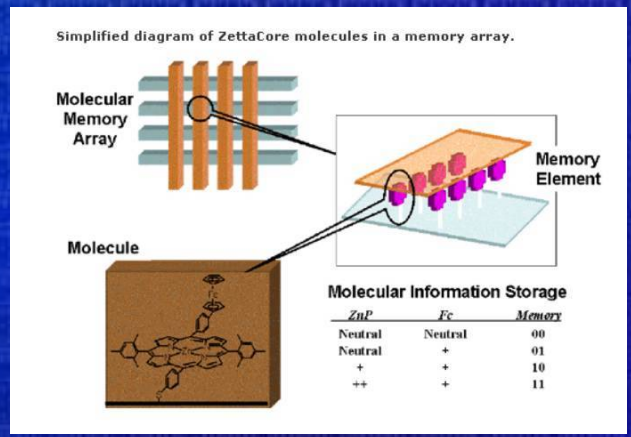

FET cell (1TJ-1T)
♦Larger cell area (>8 F²)
♦Faster random access time
♦SRAM like (≤10ns)

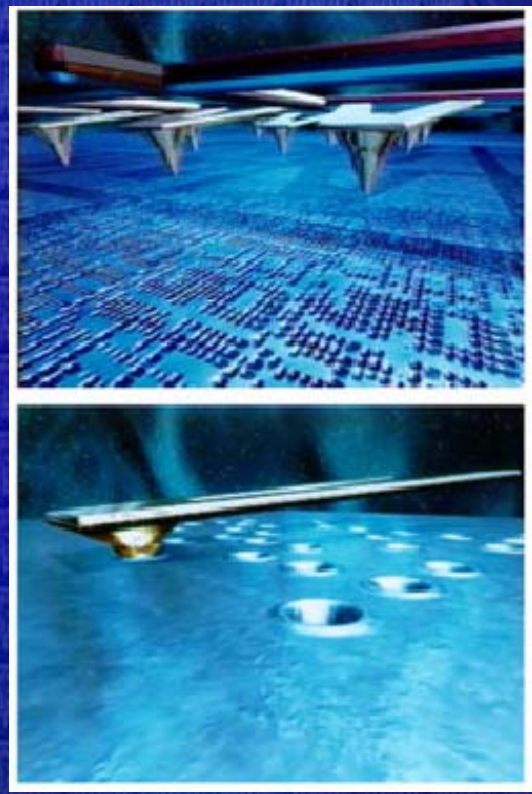

ELECTRODE
CHIP
IONS
ELECTRODE
POLYMER
POLYMER MEMORY
The plastic path to better data storage

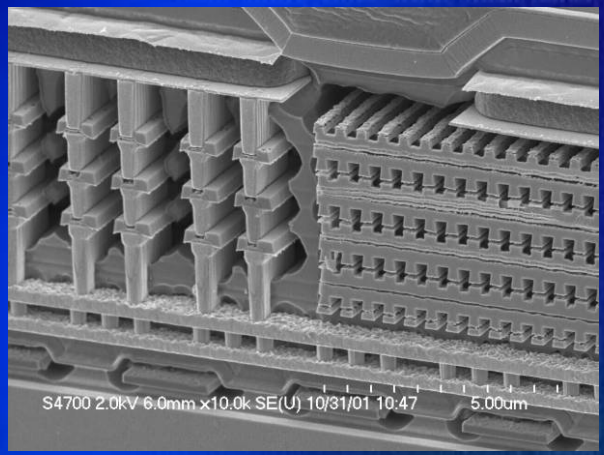

A
B
1
2
3
m
n

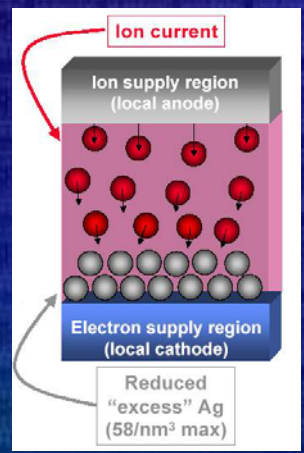

ric Field
r Atom


PCMO
Bit Line 1
Bit Line 2
Word
N+
P+
P-SILICON SUBSTRATE
Pt


Simplified diagram of ZettaCore molecules in a memory array.
Molecular Memory Array
Memory Element
Molecule
Molecular Information Storage
ZnP
Fc
Memory
Neutral
Neutral
00
Neutral
+
01
+
+
10
++
+
11




S4700 2.0kV 6.0mm x10.0k SE(U) 10/31/01 10:47
5.00um


Ion current
Ion supply region (local anode)
Electron supply region (local cathode)
Reduced "excess" Ag (58/nm³ max)

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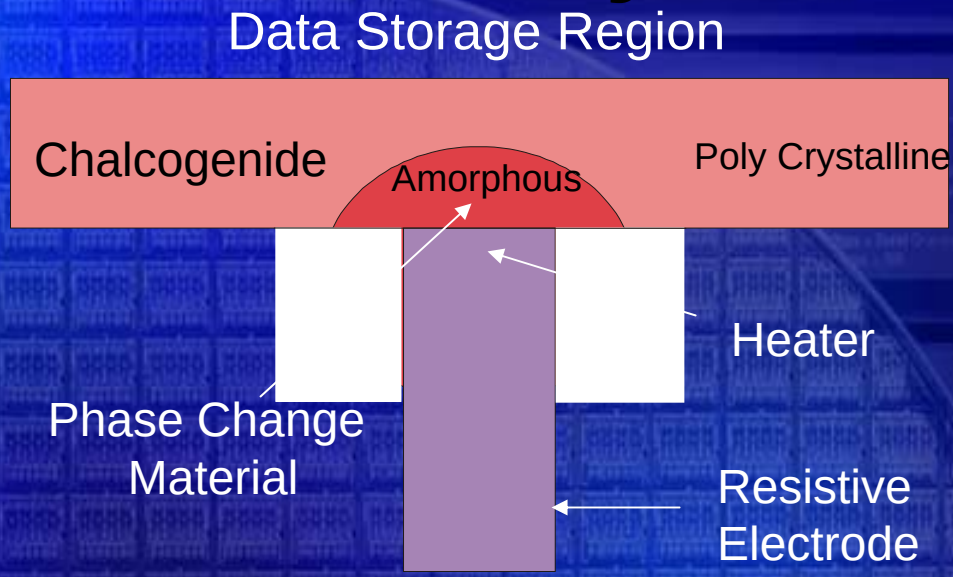
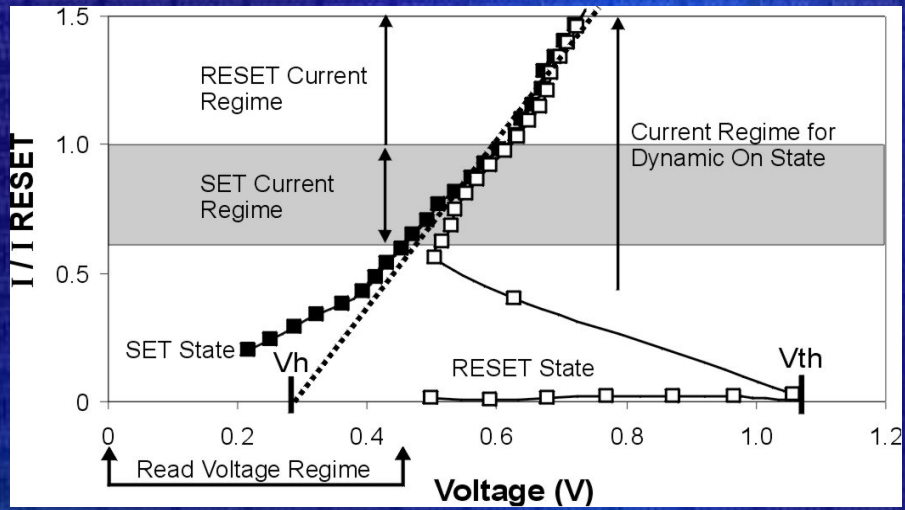
Ovonics Unified Memory

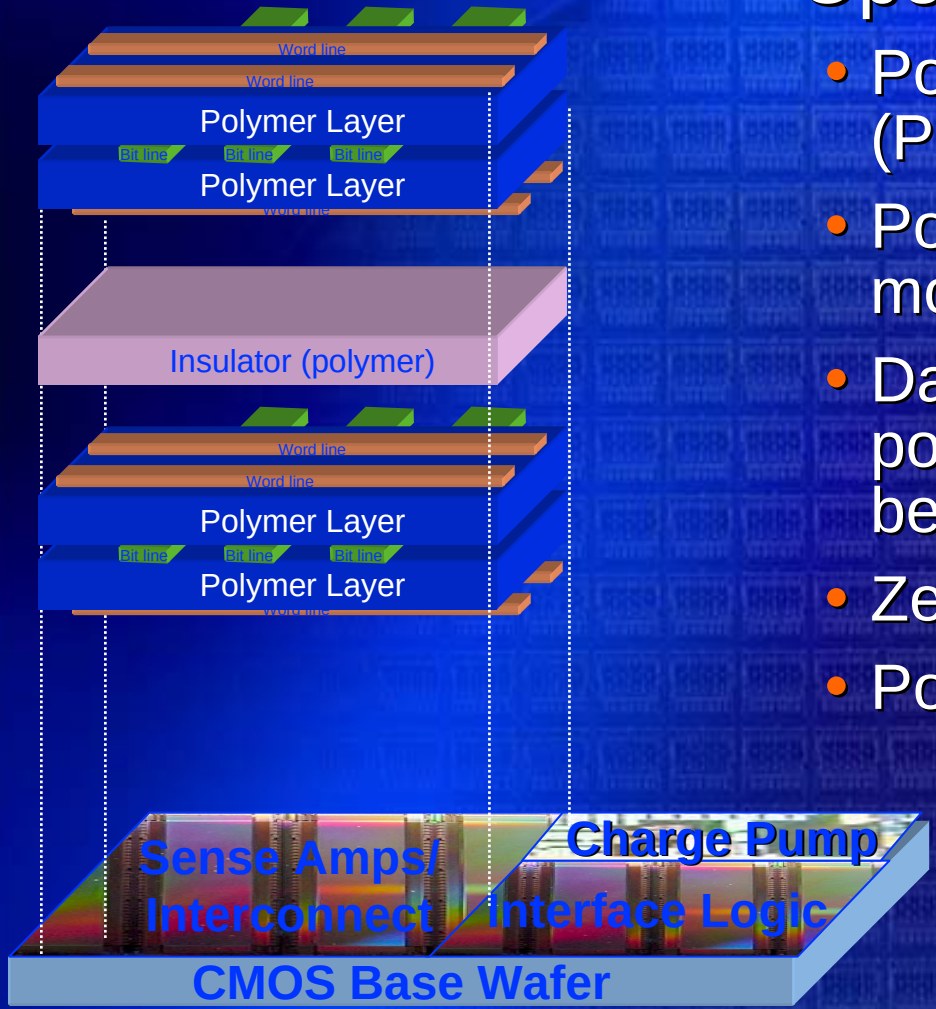
- Operation
  - Chalcogenide material alloys used in re-writable CDs and DVDs
  - Electrical energy (heat) converts the material between crystalline (conductive) and amorphous (resistive) phases
  - Cell reads by measuring resistance
  - Non-destructive read
  - ~10^{12} write/erase cycles
  - Medium write power
  - Relatively easy integration with CMOS

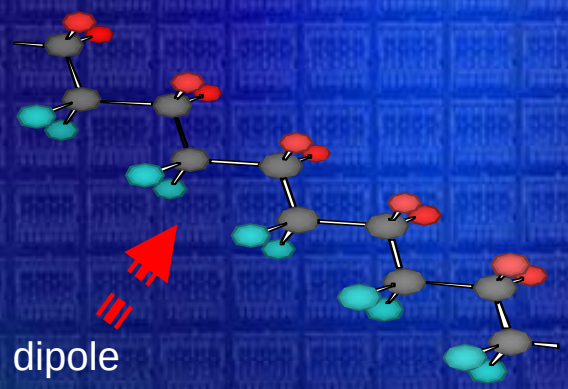




Ferroelectric Polymer Memory

- Operation
  - Polymeric Ferroelectric RAM (PFRAM)
  - Polymer chains with a dipole moment
  - Data stored by changing the polarization of the polymer between metal lines
  - Zero transistors per bit of storage
  - Polymer layers can be stacked





A Simplified View

- All above memories can be divided into two broad categories:

1. X-Y addressable, limited by lithography and follows Moore's Law
2. Seek and scan memory, no lithography, limited by scan mechanism, size and density of storage areas in storage medium

Breaking the scaling barrier

- Memory technologies requiring transistor switch will be limited in scaling -> FeRAM, MRAM; diode switch scales better -> OUM, RRAM

➔ Follows Moore's Law limited by transistor/diode

- Simple cross point switch with no transistor or diode more scalable: molecular memories

➔ Continue Moore's Law beyond transistor age

- Multi-layer memories have the potential to be lowest cost for litho defined memory

➔ Drop below historical Moore's Law

- Seek and scan can be the lowest cost but involves new memory storage and sense mechanism

➔ May go faster then Moore's Law (e.g. HDD)

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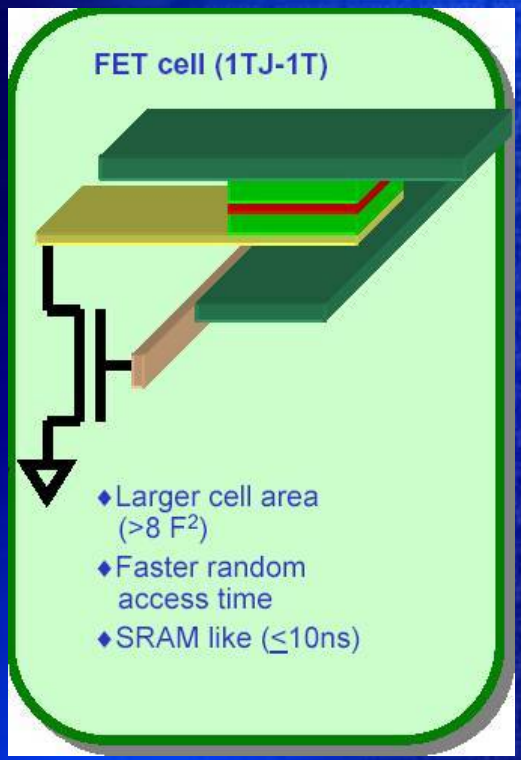
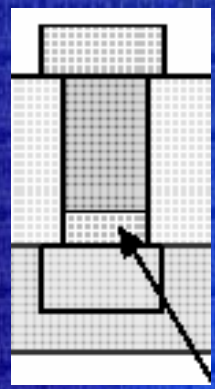
Diode switch better than transistor switch



Big



Small

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➔ Follows Moore's Law limited by transistor/diode

- **Simple cross point switch with no transistor or diode more scalable: molecular memories**

➔ **Continue Moore's Law beyond transistor age**

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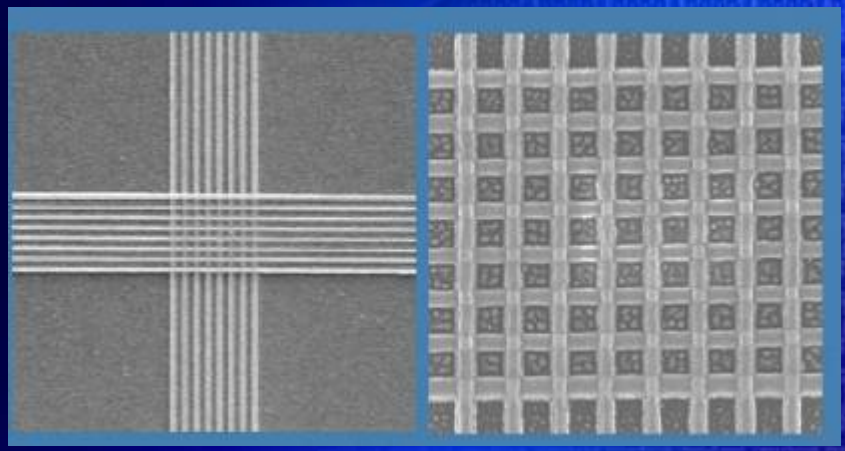
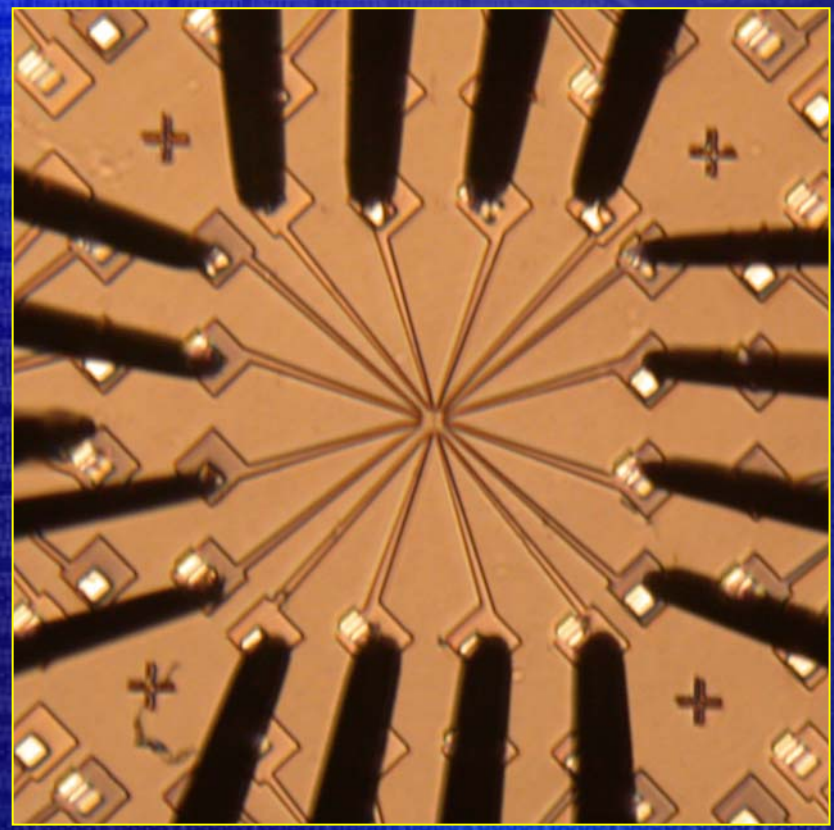
Small is not that small





- X-Y addressable memory is always limited by the limiting lithography steps: have to connect to the real world circuits
- Either self assembled circuits at the smaller geometry or new innovative architecture

Breaking the scaling barrier

- Memory technologies requiring transistor switch will be limited in scaling -> FeRAM, MRAM, diode switch scales better -> OUM, RRAM

➔ Follows Moore's Law limited by transistor/diode

- Simple cross point switch with no transistor or diode more scalable: molecular memories

➔ Continue Moore's Law beyond transistor age

- **Multi-layer memories have the potential to be lowest cost for litho defined memory**

➔ **Drop below historical Moore's Law**

- Seek and scan can be the lowest cost but involves new memory storage and sense mechanism

➔ May go faster then Moore's Law (e.g. HDD)

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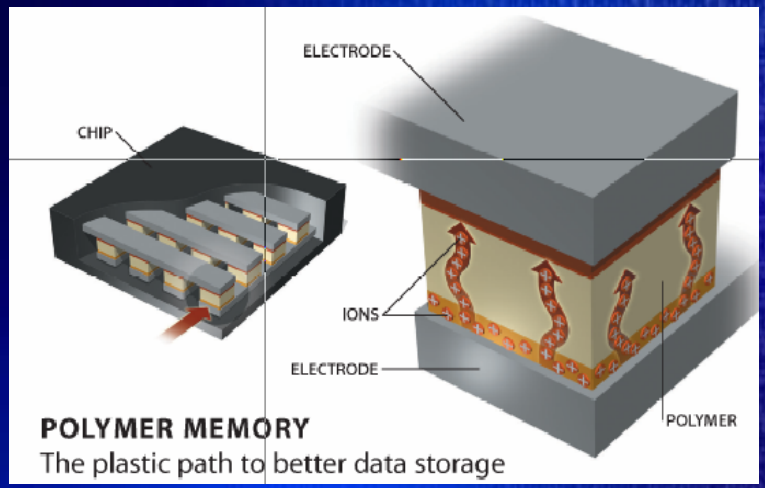
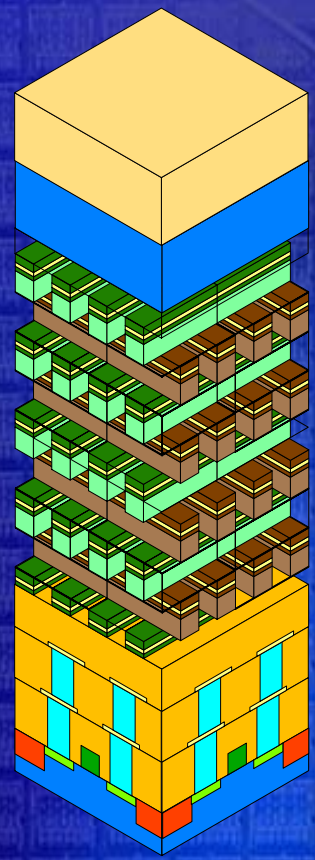
Multi-layer is smaller





Single Layer cell area = $4\lambda^2$

Multi Layer cell area = $4\lambda^2/N$ (number of layers)

Breaking the scaling barrier

- Memory technologies requiring transistor switch will be limited in scaling -> FeRAM, MRAM, diode switch scales better -> OUM, RRAM

➔ Follows Moore's Law limited by transistor/diode

- Simple cross point switch with no transistor or diode more scalable: molecular memories

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➔ **May go faster then Moore's Law (e.g. HDD)**

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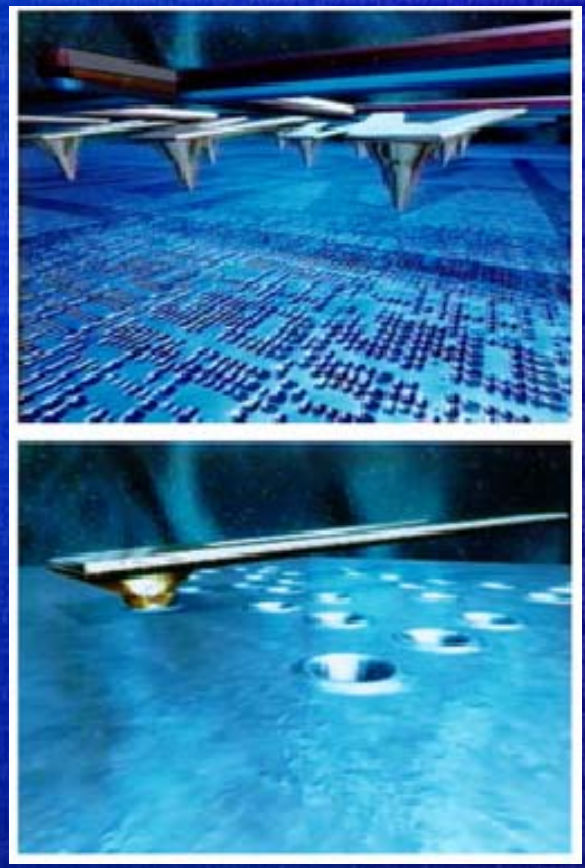
Seek and Scan has best scaling potential



Summary

- Moore's Law will continue through innovation
  - Process complexity will increase to address fundamental limits of physics
- To maintain Moore's Law cost learning curve, difficult to do it by transistor technology alone
  - New opportunity for new memory structures and new materials
- Current mainstream memory technologies of ETOX and NAND will continue to be the key technologies for more than 5 years out

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Summary (continued)

- Many potential new memory technologies
- Simple cross point memory scales better than transistor switch but will always be litho limited
- Multi-layer cross point provides lowest cost opportunities following Moore's Law
- Seek and scan memories can break through the litho barrier and scales more than Moore's Law
- System architecture integral part of memory system